THIS IS A LEGACY SPECIFICATION

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Advances in Physics

INSERT

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INSTRUCTIONS TO CANDIDATES

- This insert contains the article required to answer the questions in Section A.

INFORMATION FOR CANDIDATES

- This document consists of **8** pages. Any blank pages are indicated.

Integrated Circuit Technology

The rapid explosion of information technology in the last few decades has been made possible by the invention of the silicon chip (more commonly called an **integrated circuit** or IC) in the 1960s. Before this time, all circuits were made by hand with individual components that were connected together with wires. Apart from being expensive to produce, the circuits were bulky and less reliable than modern integrated circuits. The external and internal pictures of the mobile phone in Fig. 1 below show how small appliances can be made using ICs.

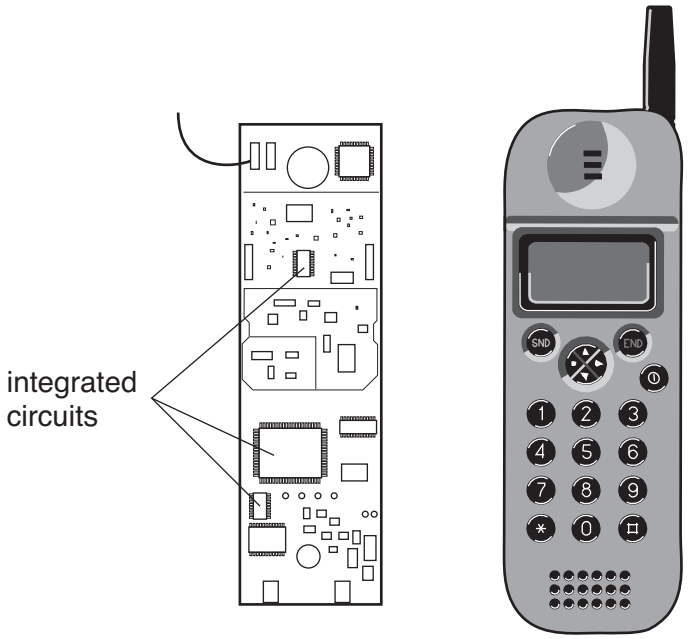

Fig. 1

Producing pure single-crystal silicon

An IC is a complete circuit of components and connecting tracks, which is imprinted onto the surface of a thin, brittle slice of silicon crystal about the size of a finger nail. Purified silicon is a covalently-bonded, polycrystalline material. This is not suitable for making an IC, the circuit of which must be on one single crystal.

The first stage of the manufacturing process therefore involves the creation of a long rod of single crystal silicon. First, a graphite crucible, surrounded by coils carrying high-frequency alternating current, is used to melt the lumps of solid silicon (Fig. 2).

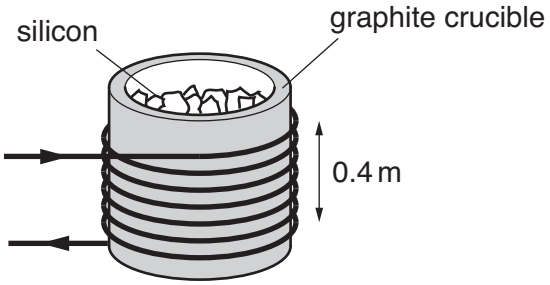

Fig. 2

The high-frequency coil, 0.4 m in length and consisting of 7 turns of thick wire, carries an alternating current with a peak value of about 1100 A oscillating at 10 kHz. The resulting oscillating magnetic field induces an emf directly into the crucible, both in the graphite wall and in the silicon contents.

The crucible acts as a one-turn secondary coil, and the resulting eddy current heats the graphite. This mechanism of energy transfer is extremely efficient as it does not rely on conduction from a heat source to the crucible and as a result the silicon in the crucible very quickly reaches its melting point 1700 K.

Next, a seed crystal, a single crystal of pure silicon a few millimetres across, is dipped into the molten silicon. The seed crystal is very slowly pulled away from the surface of the liquid and atoms of silicon solidify onto it in the same repetitive pattern. In this way the seed crystal structure is grown into a single crystal ingot about 1 m long and 20 cm in diameter. Fig. 3A shows a cross section of this process.

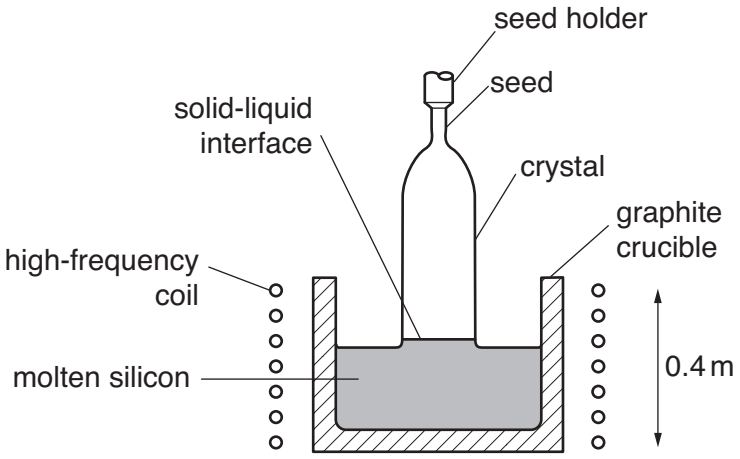

Fig. 3A

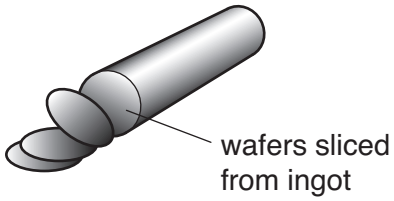

Fig. 3B

The ingot is then sawn into thin circular discs ('wafers') about 20 cm in diameter and less than 1 mm thick (see Fig. 3B above). One ingot will form hundreds of silicon wafers of the highest purity.

Making integrated circuits

Crystalline silicon is a semiconductor material with an electrical conductivity much smaller than a metal but much higher than an insulator (Fig. 4).

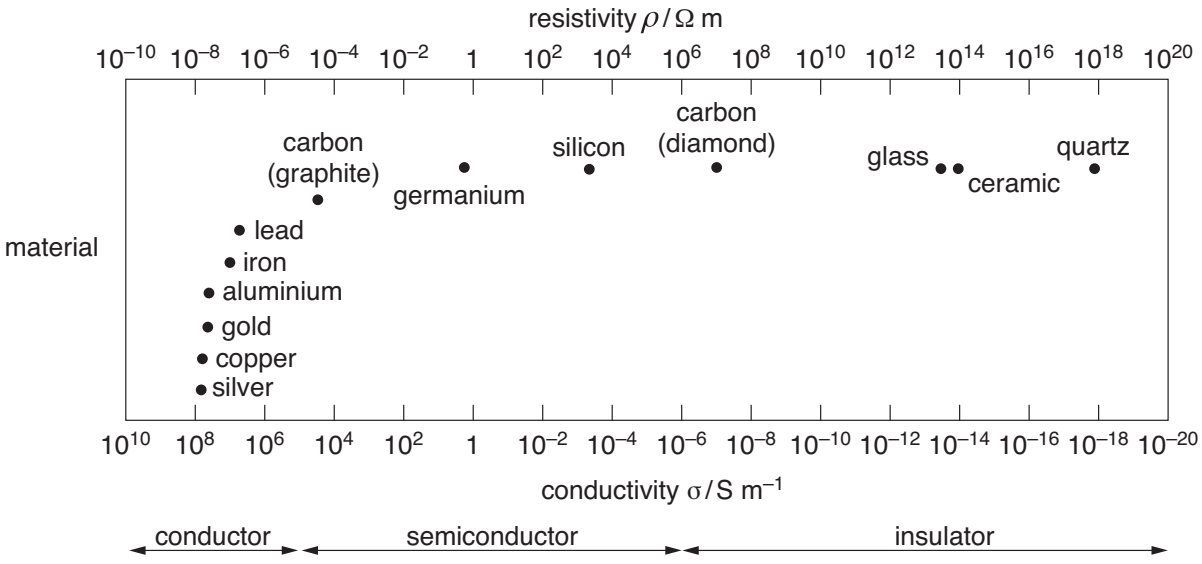

Fig. 4

Although pure silicon does not have many free electrons to allow conduction to take place readily, the addition of small quantities of other elements such as phosphorus or boron, referred to as 'foreign atoms', causes the conducting properties of the crystal to change. Adding foreign atoms into the pure crystal is called **doping**, and it is this that allows different electrical components to be constructed in the silicon wafer. The doping atoms must be implanted in precise locations on the IC in order that each component is correctly placed in the circuit.

To ensure that the doping atoms are implanted at the right locations, a layer of insulating material (lacquer) is first applied across the whole surface of the silicon. This acts a barrier to implantation and can be selectively removed if light is allowed to fall on to the lacquer.

Next, a **mask** containing opaque regions with transparent gaps is created. This allows an image of the circuit to be projected onto the wafer. The mask, which acts in a similar way to an artist's stencil, is placed above the lacquer-coated wafer. Wherever there is a gap in the mask, the lacquer will be exposed to light, which chemically changes the exposed lacquer. By moving the silicon slice under the mask, many small copies of the original mask can be printed onto the same slice. This method cannot be used to make extremely tiny copies of the mask, however. The area of lacquer exposed is generally somewhat larger than the 'shadow' of the mask, because the light spreads by diffraction. This is more easily shown in the simplified version of the process of Fig. 5 A, using parallel incident light. The exposed lacquer is chemically changed, which allows it to be washed away, exposing pure silicon (Fig. 5 B). These are the areas into which doping atoms will be implanted, as shown in Fig. 5 C.

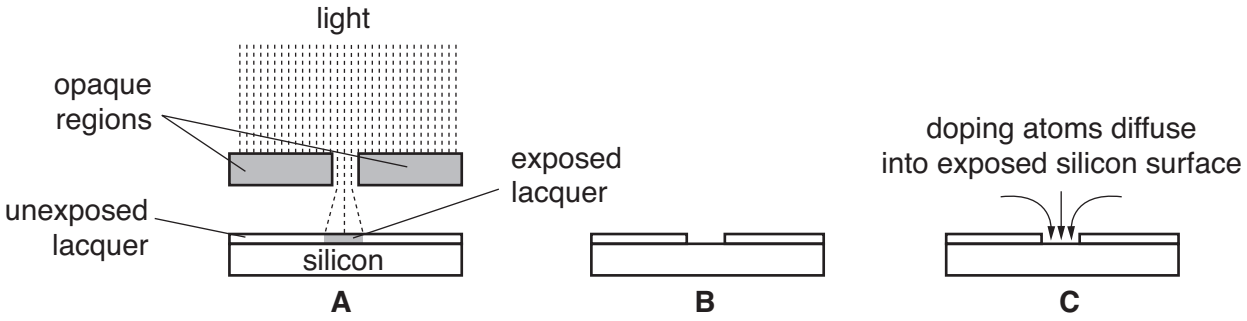

Fig. 5

Doping atoms in the form of a hot gas are introduced into the silicon wafer by diffusion in an oven. Although diffusion occurs at all temperatures, the rate at which gases diffuse into solids is normally extremely low. In order for a foreign atom, such as phosphorus, to move from one silicon lattice site to another, an activation energy E_A, typically 3 to 4 eV (about 6×10^{-19} J), must be supplied. As a result of the activation energy needed for each atom to move, the diffusion rate increases according to the Boltzmann factor. To increase diffusion as much as possible, this process takes place in an oven at a temperature of around 1300 K, as high a temperature as is possible for the silicon wafer to remain crystalline. This roughly four-fold increase in temperature over room temperature speeds up the process by a huge factor. The high temperature doping gas flows over the wafer surface, and atoms diffuse a few micrometres into the silicon surface. After the removal of the remaining unexposed lacquer, there are now tiny islands of doped silicon embedded within pure silicon across the whole surface of the silicon wafer.

The lacquer and mask process is repeated to form the pattern of connecting tracks that join all the components together. A metal such as aluminium or, more recently, copper, is vaporised onto the surface and will solidify only where the tracks have been defined by the mask.

In practice, many identical copies of the whole circuit will have been repeated over the surface of a single wafer of silicon (Fig. 6A). The circular wafer is now cut into rectangular chips each with a copy of the entire circuit. These chips are each mounted on a block of plastic and the internal tracks on the silicon surface are connected by very fine gold wires to the metal legs that emerge from the package (Fig. 6B). The chip is covered with a protective layer of plastic before it is ready to be connected, by the metal legs, to other components in a larger circuit.

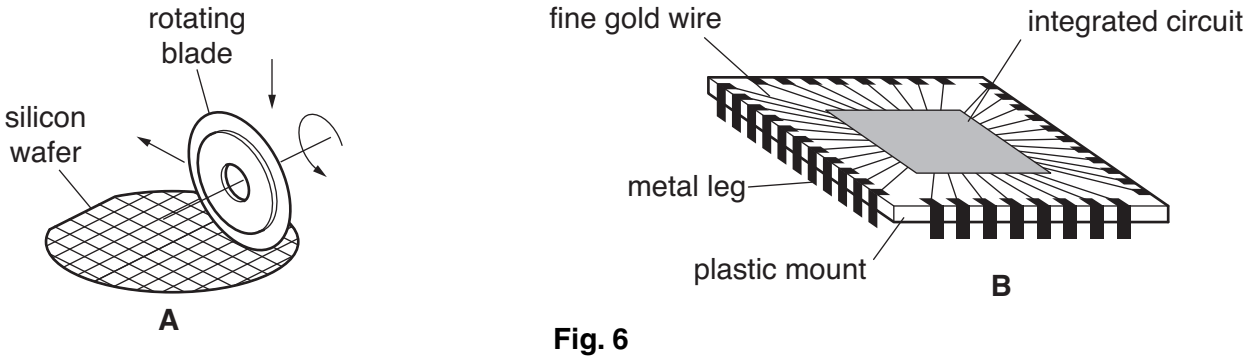

Fig. 6

Moore's Law

At the heart of every computer is the Central Processor Unit (CPU) that performs the arithmetical functions. The CPU is a large integrated circuit containing many millions of transistors. Each transistor is a digital switch and can be turned on (binary 1) or off (binary 0) as required. As the technology of chip manufacture has been refined over the last thirty years the size of each transistor has been greatly reduced. This has enabled computers to become ever faster and more powerful year on year. In 1960 a transistor on an integrated circuit was about 20 μm long and 20 μm wide and by 2000 these dimensions had been reduced to about 0.2 μm. This represents a reduction in linear size of about 11% each year. In other words the length of a typical transistor at the end of a year is only 89% of its size at the start. In 1965 Gordon Moore, co-founder of the CPU manufacturer Intel, made a prediction, now known as Moore's Law, that the number of transistors per CPU would double every two years. So far he has been more or less correct as shown by the graph in Fig. 7.

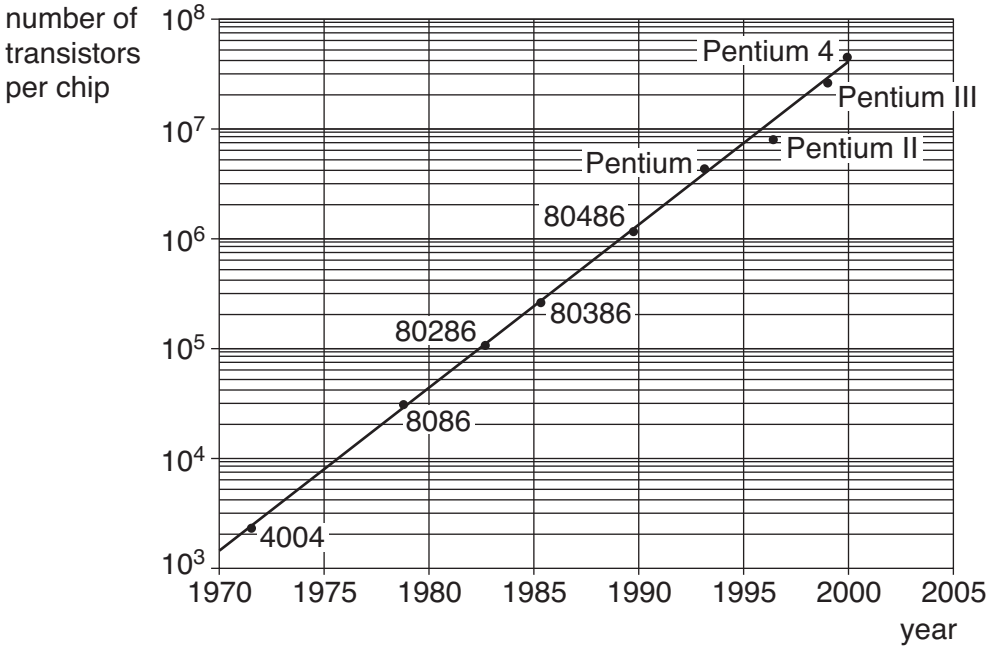

Fig. 7

The increase in the number of transistors on a single chip, typically of area about 1 cm^2, has come about mainly from the shrinking size of each transistor.

Problems in making smaller ICs

In order for Moore's Law to continue to be true, we must continue to make integrated circuit components still smaller, but there are a number of technical difficulties to overcome before achieving this goal.

Firstly, the masks used to imprint the circuit detail onto the silicon must be made with smaller gaps. Technologists are now trying to imprint details on a chip surface that are comparable with the wavelength of ultraviolet light. However, when the ultraviolet shines through the mask, diffraction exposes too large an area of the lacquer below, as shown in Fig. 5A. So unfortunately, reducing the wavelength further using other electromagnetic waves is not feasible. For this reason, the use of streams of electrons instead of photons has been proposed for the future. With this **electron beam lithography** technique it is believed that transistor dimensions of around 0.08 μm could be expected soon.

A second problem associated with reducing the size of components on a chip is the increased resistance of the interconnecting metal tracks. If each linear dimension is halved, then the track resistance doubles as a result. This problem has been reduced recently by using copper, which has a resistivity approximately half that of the aluminium previously used.

In addition to resistance problems, adjacent pairs of parallel tracks behave like a parallel plate capacitor (Fig. 8).

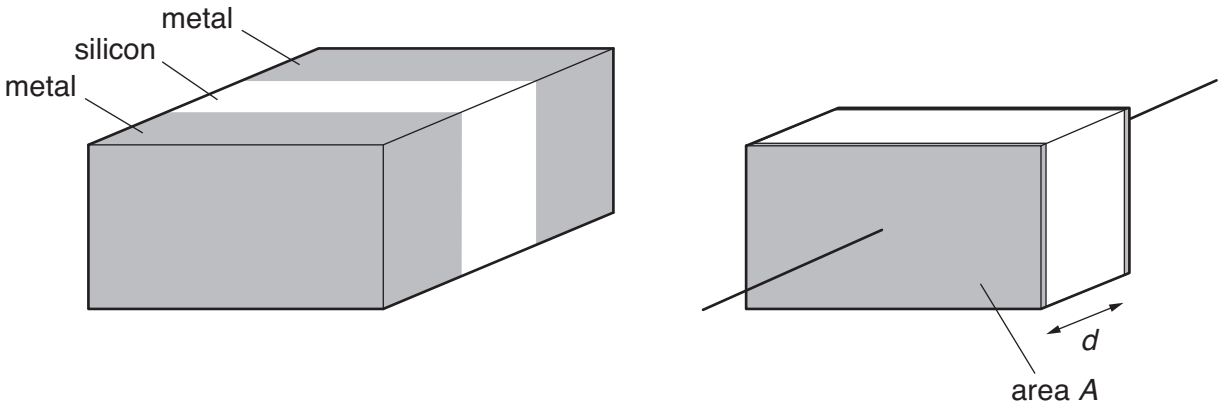

Fig. 8

The capacitance of a pair of parallel plates, each of area A, separated in vacuum by a distance d, is given by

$$C = \varepsilon_0 \frac{A}{d}$$

where ε_0 is a fundamental constant known as the permittivity of free space. If the plates are separated by a material and not a vacuum, the constant ε_0 is increased by a factor ε_r, which is known as the **relative permittivity** of the material, giving

$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$. For silicon, the relative permittivity $\varepsilon_r = 2.4$.

The added resistance and capacitance in the circuit can make the propagation of signals around the chip much slower. This can be a problem for the Central Processor Unit (CPU) chip in a computer when large amounts of data need to be transported in short time intervals. If a computer is processing a video file, for example, it has to handle 25 frames each second, with each frame containing at least 30 kilobytes of information. Even this can only be achieved using massive data compression (for example, by transmitting only the pixels that change from one frame to the next).

It has been proposed that, instead of reducing the size of all the components on the chip, it may be better to stack chips into a three-dimensional pile that makes a cubic structure. Research into this technique has, however, highlighted difficulties in allowing heat to escape from the chip. Some scientists are predicting that the silicon chip is nearly at the limit of its capabilities and that new technologies using different materials will have to be developed in the future if Moore's Law is to apply for much longer.

END OF ARTICLE